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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/004,458	10/23/2001	Thomas Fung	2875.0440001	6843

26111 7590 03/11/2010

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EXAMINER	
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ART UNIT	PAPER NUMBER
2437	

MAIL DATE	DELIVERY MODE
03/11/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/004,458	FUNG ET AL.	
	Examiner	Art Unit	
	JEFFREY D. POPHAM	2437	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 December 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,8-12,14-16,18,22-24 and 26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,8-12,14-16,18,22-24 and 26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 September 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Remarks

Claims 1-4, 8-12, 14-16, 18, 22-24, and 26 are pending.

Response to Arguments

1. Applicant's arguments filed 12/22/2009 have been fully considered but they are not persuasive.

Applicant argues that Wang does not disclose that "moving the first interrupt indicator comprises setting the first interrupt indicator associated with the first control record to disabled and setting the second interrupt indicator associated with the second control record to enabled". Along with this, Applicant argues that "Even if we assume for the sake of argument that the done flags disclosed in Wang are comparable to the interrupt indicators in claim 1...". It is first noted that Wang was not stated as disclosing interrupt indicators, but rather, Bashford was. Wang discloses use of retirement indicators, as can be seen throughout the patent. There are multiple flags and bits being used within Wang to specify when an instruction is retirable. As discussed in column 10, lines 12-20, an external write enable bit will be set for a current instruction when in all previous instructions have been completed and the current instruction completes processing, thereby allowing the instruction to be retired. As discussed in column 10, lines 21-32, instructions completed out of order are stored in temporary buffer until all previous instructions are completed. Until all previous instructions are completed, these instructions cannot be retired (unretirable). The done flag is used in the done block (420) to specify which instructions have

been completed but cannot yet be retired (are unretirable). As discussed above, when an instruction can be retired, the external write enable bit is set and it is written to register array 404. In this situation, the done flag is not set in the done block, as the instruction has been completed in order. As one can see, the storing of a done flag for a particular instruction in the done block shows that the instruction has completed processing but cannot be retired. This is equivalent to disabling a retirement indicator, as this done flag explicitly states that this instruction cannot yet be retired, as other instructions prior to it have not been retired. When the instruction(s) prior to this instruction for which the done flag is set are completed, it's external write enable bit is set, allowing it to be written to register array 404. Once this is done for all instructions prior to the instruction for which the done flag is set, the instruction for which the done flag is set is then allowed to be retired and is enabled to be written/retired to the register array 404. Although not explicitly using the terminology of enabling and disabling an indicator, one of ordinary skill in the art will note the correspondence between allowing retiring and disallowing retiring of an instruction via use of flags and bits to correspond to enabling and disabling of an indicator that allows or disallows retiring of the instruction.

Looking at the above, with respect to 2 instructions, one can see from column 10, lines 12-20, that, when the instructions are completed in order, the external write enable bit is set, allowing the instruction to be retired to the register array. When the instructions are completed out of order, however (e.g. numerically sequential instruction 1 is still processing while instruction 2 has

completed processing), the done flag for instruction 2 is set, marking instruction 2 as unretirable (retiring is disabled). Once instruction 1 has completed processing, instruction 1 will have the external enable write bit set, thus marking it retirable, and will be written (retired) to the register array. As one can see, Wang teaches setting the first retirement indicator associated with the first (younger in this limitation) control record, corresponding to instruction 2 in the example above, to disabled by setting the done flag, which is only performed when out of order completion occurs, thereby marking instruction 2 as unretirable. Then, when instruction 1 completes (being associated with the older control record in this limitation), the external write enable bit is set, thereby marking instruction 1 as retirable. Once this is done, instruction 2 is also retirable and may be retired simultaneously with, or sequential to, instruction 1. As can be seen, the combination of the external write enable bit and done flag clearly describes a retirement indicator, that indicates when an instruction is retirable. Bashford teaches the fact that, when instructions are retirable, an interrupt is generated, thereby showing that the retirement indicator of Wang is an interrupt indicator in the combination of Wang in view of Bashford.

Claim Objections

2. Claim 18 is objected to because of the following informalities: Claim 18 recites "wherein moving the first interrupt indicator associated with the first control record onto the second control record..". However, claim 15, from which claim 18 depends, specifies such moving as the first indicator being "moved onto

a second interrupt indicator associated with the second control record". Therefore, in order to provide proper antecedent basis, the portion cited above from claim 18 has been construed as "wherein moving the first interrupt indicator associated with the first control record onto the second interrupt indicator associated with the second control record". Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 3, 4, 8-12, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang (U.S. Patent 6,412,064) in view of Bashford (U.S. Patent 6,629,179).

Regarding Claim 1,

Wang discloses a method for processing data using a plurality of processing engines, the method comprising:

Processing first data associated with a first control record in a first processing engine (Abstract; Column 5, lines 58-64; and Column 7, lines 22-52; executing/processing instructions in the functional units, such as the ALUs);

Processing second data associated with a second control record in a second processing engine, wherein the first and second data are processed in parallel (Abstract; Column 5, lines 58-64; and Column 7, lines 22-52; such executing/processing of instructions being done simultaneously, as noted by sending multiple instructions in the same clock cycle to different functional units and/or the out-of-order processing and completion);

If processing of the first data completes before processing of the second data completes and the first control record is younger than the second control record, moving a first retirement indicator associated with the first control record onto a second retirement indicator associated with the second control record, wherein moving the first retirement indicator comprises setting the first retirement indicator associated with the first control record to disabled and setting the second retirement indicator associated with the second control record to enabled (Abstract; and Column 10, lines 21-61; write enable signal 604, for example, which is enabled when writes to register array are allowed (writing to register array is only allowed when the instruction is retirable, meaning that all previous instructions have completed processing); in this situation, the system allowed for simultaneous retiring and, thus, enabling writing to the register array, of groups of parallel-

processed data, as discussed in column 10, lines 31-32, for example);

If processing of the first data completes before processing of the second data completes and the first control record is older than the second control record, retiring the instruction by writing it directly to the register array (or, possibly, by first going to the temporary buffer and then to the register array), such retiring/writing being performed before processing of the second data completes (Abstract; and Column 10, lines 12-20); and

In-order generation of exceptions, such that all previous instructions are completed before an exception for an instruction is generated (Column 5, lines 30-47);

But does not explicitly disclose that the retirement indicators comprise interrupt indicators.

Bashford, however, discloses that retirement indicators comprise interrupt indicators (Abstract; Column 2, line 47 to Column 3, line 9; and Column 6, lines 42-56; completion interrupts that are only generated once all prior transactions (corresponding to the instructions of Wang in the combination) have completed); and

Generating an interrupt when processing of the first data completes in proper order and is ready for retirement (Abstract; Column 2, line 47 to Column 3, line 9; and Column 6, lines 42-56).

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to incorporate the interrupt generating device of Bashford into the parallel processing system of Wang in order to allow the system to generate interrupts upon completion of instructions, thereby explicitly informing a host processor of the completion of each instruction, and/or to allow for the expansion of out-of-order execution with ordered responses described by Wang to additional devices over buses, thereby obtaining the benefits of proper ordering while allowing for parallel processing on many various devices (e.g. hard drives, I/O devices, etc.).

Regarding Claim 3,

Wang as modified by Bashford discloses the method of claim 1, in addition, Bashford discloses that moving the first interrupt indicator comprises determining that the first interrupt indicator is enabled (Abstract; Column 2, line 47 to Column 3, line 9; and Column 6, lines 42-56; in at least some embodiments of Bashford, interrupts are provided for completion of all operations, therefore, the indicator will be enabled since an interrupt is intended to be generated after completion of the operation, only being disabled when the operation finishes early and the interrupt must be delayed).

Regarding Claim 4,

Wang as modified by Bashford discloses the method of claim 1, in addition, Bashford discloses that moving the first interrupt indicator comprises delaying the generation of an interrupt associated with the first control record (Column 6, lines 42-56; and Column 9, lines 35-50).

Regarding Claim 8,

Wang as modified by Bashford discloses the method of claim 1, in addition, Bashford discloses that the first control record comprises a reference to data (Column 6, line 54 to Column 7, line 10; and Column 9, lines 6-30, for example, showing instruction dependencies and tags referring to data, respectively).

Regarding Claim 9,

Wang as modified by Bashford discloses the method of claim 8, in addition, Wang discloses that the first control record comprises a reference to an operation to be performed on data (Column 5, lines 49-64, for example, showing integer and floating-point operations).

Regarding Claim 10,

Wang as modified by Bashford discloses the method of claim 1, in addition, Wang discloses writing processed data to memory associated with a host (Abstract; and Column 10, lines 12-61).

Regarding Claim 11,

Wang as modified by Bashford discloses the method of claim 10, in addition, Bashford discloses that the host is an external processor coupled to the processing engines (Figure 1; Host CPU and Chipset corresponding to the host as an external processor).

Regarding Claim 12,

Wang as modified by Bashford discloses the method of claim 11, in addition, Bashford discloses that the external processor is coupled to the processing engines through a scheduler (Figure 1; PCI bridge corresponding to scheduler).

Regarding Claim 14,

Wang as modified by Bashford discloses the method of claim 12, in addition, Wang discloses that a processor reads the processed data when the data is retired (Column 8, lines 18-33; providing data stored in the register array to a functional unit); and Bashford discloses that the data would be received by the external processor when the interrupt is generated (Abstract; Column 2, line 47 to Column 3, line 9; and Column 6, lines 42-56).

4. Claims 2, 15, 16, 18, 22-24, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang in view of Bashford, further in view of Pierson (Pierson et al., "Context-Agile Encryption for High Speed Communication Networks", Computer Communications Review, Association for Computing Machinery, Vol. 29, No. 1, January 1999, pp. 35-49).

Regarding Claim 2,

Wang as modified by Bashford does not explicitly disclose that the first processing engine is a public key engine.

Pierson, however, discloses that the first processing engine is a public key engine (Pages 46-48, Section 5.2). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to incorporate the cryptographic system of Pierson into the parallel processing system of Wang as modified by Bashford in order to allow the system to perform encryption and authentication, thereby providing additional security, and/or to provide such encryption and authentication quickly and easily, encrypting multiple communications (with different keys, algorithms, etc.) at a time without the normal delay required for context switching.

Regarding Claim 15,

Wang discloses an apparatus comprising:

A first processing engine configured to process a first control record (Abstract; Column 5, lines 58-64; and Column 7, lines 22-52);

A second processing engine configured to process a second control record, wherein the first and second processing engines are configured to process the first and second control records in

parallel (Abstract; Column 5, lines 58-64; and Column 7, lines 22-52);

A history buffer configured to retain information associated with the first and second control records including a first retirement indicator associated with the first control record and a second retirement indicator associated with the second control record (Abstract; Column 8, lines 18-29; and Column 10, lines 4-44; temporary buffer);

Wherein the history buffer is configured to move the first retirement indicator associated with the first control record onto a second retirement indicator associated with the second control record if processing of the first control record completes before processing of the second control record completes and the first control record is younger than the second control record (Abstract; and Column 10, lines 21-61);

Retiring an instruction if processing of the first control record completes before processing of the second control record completes and the first control record is older than the second control record, the retiring configured to occur before processing of the second control record completes (Abstract; and Column 10, lines 12-20); and

In-order generation of exceptions, such that all previous instructions are completed before an exception for an instruction is generated (Column 5, lines 30-47);

Wherein moving the first retirement indicator comprises setting the first retirement indicator associated with the first control record to disabled and setting the second retirement indicator associated with the second control record to enabled (Abstract; and Column 10, lines 21-61);

But does not explicitly disclose that the apparatus is a cryptography accelerator or that the retirement indicators comprise interrupt indicators.

Bashford, however, discloses that retirement indicators comprise interrupt indicators (Abstract; Column 2, line 47 to Column 3, line 9; and Column 6, lines 42-56); and

Generating an interrupt when processing of the first data completes in proper order and is ready for retirement (Abstract; Column 2, line 47 to Column 3, line 9; and Column 6, lines 42-56). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to incorporate the interrupt generating device of Bashford into the parallel processing system of Wang in order to allow the system to generate interrupts upon completion of instructions, thereby explicitly informing a host processor of the completion of each instruction, and/or to allow for the expansion of

out-of-order execution with ordered responses described by Wang to additional devices over buses, thereby obtaining the benefits of proper ordering while allowing for parallel processing on many various devices (e.g. hard drives, I/O devices, etc.).

Pierson, however, discloses that the apparatus is a cryptography accelerator (Pages 46-48, Section 5.2). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to incorporate the cryptographic system of Pierson into the parallel processing system of Wang as modified by Bashford in order to allow the system to perform encryption and authentication, thereby providing additional security, and/or to provide such encryption and authentication quickly and easily, encrypting multiple communications (with different keys, algorithms, etc.) at a time without the normal delay required for context switching.

Regarding Claim 16,

Wang as modified by Bashford and Pierson discloses the apparatus of claim 15, in addition, Pierson discloses that the first processing engine is a public key engine (Pages 46-48, Section 5.2).

Regarding Claim 18,

Wang as modified by Bashford and Pierson discloses the apparatus of claim 15, in addition, Bashford discloses that moving

the first interrupt indicator associated with the first control record onto the second interrupt indicator associated with the second control record further comprises delaying the generation of an interrupt associated with the first control record (Column 6, lines 42-56; and Column 9, lines 35-50).

Regarding Claim 22,

Wang as modified by Bashford and Pierson discloses the apparatus of claim 15, in addition, Bashford discloses that the second control record comprises a reference to data (Column 6, line 54 to Column 7, line 10; and Column 9, lines 6-30).

Regarding Claim 23,

Wang as modified by Bashford and Pierson discloses the apparatus of claim 22, in addition, Wang discloses that the second control record comprises a reference to an operation to be performed on data (Column 5, lines 49-64).

Regarding Claim 24,

Wang as modified by Bashford and Pierson discloses the apparatus of claim 23, in addition, Bashford discloses an external processor coupled to the processing engines through a scheduler (Figure 1).

Regarding Claim 26,

Wang as modified by Bashford and Pierson discloses the apparatus of claim 24, in addition, Wang discloses that a processor

reads the processed data when the data is retired (Column 8, lines 18-33; providing data stored in the register array to a functional unit); and Bashford discloses that the data would be received by the external processor when the interrupt is generated (Abstract; Column 2, line 47 to Column 3, line 9; and Column 6, lines 42-56).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JEFFREY D. POPHAM whose telephone number is (571)272-7215. The examiner can normally be reached on M-F 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Emmanuel Moise can be reached on (571)272-3865. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jeffrey D Popham
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